

Use of nano-scale double-gate MOSFETs in low-power tunable current mode analog circuits

Hesham F. A. Hamed[✉] · Savas Kaya[✉]
Janusz A. Starzyk

Received: 6 June 2007 / Revised: 6 June 2007 / Accepted: 17 January 2008
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Abstract Use of independently-driven nano-scale double gate (DG) MOSFETs for low-power analog circuits is emphasized and illustrated. In independent drive configuration, the top gate response of DG-MOSFETs can be altered by application of a control voltage on the bottom gate. We show that this could be a powerful method to conveniently tune the response of conventional CMOS analog circuits especially for current-mode design. Several examples of such circuits, including current mirrors, a differential current amplifier and differential integrators are illustrated and their performance gauged using TCAD simulations. The topologies and biasing schemes explored here show how the nano-scale DG-MOSFETs may pave way for efficient, mismatch-tolerant and smaller circuits with tunable characteristics.

Keywords Integrated circuits · Tunable analog circuits · Current mode circuits · Mixed-mode simulations · DG-MOSFET

1 Introduction

In low-power analog systems, current-mode signal processing has been usually considered an attractive strategy due to its potential for high-speed operation and low-voltage compatibility [1, 2]. These features can be

especially rewarding in the context of mixed-signal system design in sub-100 nm CMOS era, where SOI substrates provide a viable platform for active and passive RF device integration while also hosting ultra-small CMOS devices for the digital system blocks. However, in most current-mode circuits, the tuning of circuit response is achieved by use of extra transistors, leading to losses in area and performance. Moreover, device mismatch can lead to significant reduction in the circuit performance. In the present work, we explore novel low-voltage analog circuits using double-gate (DG) MOSFETs, which provide means to alleviate above concerns by utilizing the new architectural features and operational modes of these nano-scale transistors.

Originally proposed as an ideal solution to silicon roadmap downscaling concerns, the DG-MOSFET has vast potential also in analog circuit applications as a four-terminal device, where its response may be conveniently tuned via secondary gate bias [3, 4]. Due to their ability to effectively handle GHz modulation, to minimize parasitics via low-loss SOI substrate and to cross-modulate dual gates through thin silicon body, these nano-transistors are strong contenders for highly-integrated analogue RF systems in lucrative wireless communications market. However, their RF potential has not been assessed accurately or extensively: there is a clear gap in the literature with regards to analog circuit applications [5]. We explore this gap in this work, surveying and exploiting unique features of DG-MOSFET's especially within current-mode design framework [6, 7].

Besides, tunable functionality, the following circuits provide additional gains in terms of area, power and parasitics (i.e. speed). This is achieved by using DG-MOSFET in independently driven mode (IDDG) where the two gates are physically separated and biased

H. F. A. Hamed (✉) · S. Kaya · J. A. Starzyk
School of Electrical Engineering and Computer Science,
Ohio University, Athens, OH 45701, USA
e-mail: hfah66@yahoo.com

S. Kaya
e-mail: kaya@ohio.edu

differently, as opposed to symmetrically-driven (SDDG) counterparts used typically in digital applications to maximize I_{ON}/I_{OFF} ratio [7, 8]. Consequently, it is possible to build high-performance and low-voltage mixed-signal systems using DG-MOSFET devices with added benefit of tunable analog characteristics as well as reconfigurable logic functionality. This is especially valuable at a time when performance enhancement via device scaling becomes exceedingly expensive and difficult, and innovative circuit engineering is sought to elongate the dominance of Si technology [1]. Although several works that utilizes DG-MOSFETs in RF mixing applications have been published so far [8–10], the tunability of the DG-MOSFETs have been largely ignored by the analog designers. In the present work, we will explore several simple analog circuit blocks built using DG-MOSFETs, in which bottom gate is used to tune circuit performance. We will show how compact low-power circuits including current mirrors, a differential current amplifier and differential integrators may be built and tuned using TCAD simulations. Consequently we provide valuable insights into novel analog design strategies and circuits based on DG-MOSFETs.

1.1 Device structure and modeling

DG-MOSFETs considered in this work are chosen to facilitate the mixed-mode circuit design methodology, which seeks to integrate analog circuits on the same substrate as digital building blocks with minimal overhead to

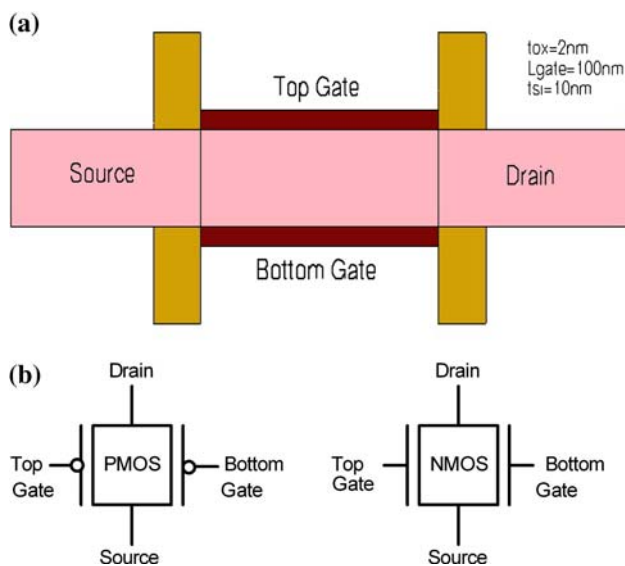


Fig. 1 (a) The DG-MOSFET device structure used in this work has a gate length $L_g = 100$ nm, a body thickness $t_{si} = 10$ nm and oxide thickness $t_{ox} = 2$ nm, typical values for those digital applications. (b) DG-MOSFET circuit symbols

the fabrication sequence. This implies using DG-MOSFETs with a minimal body thickness ($t_{si} \leq 30$ nm), oxide insulator thickness ($t_{ox} \leq 5$ nm) and gate length ($L \leq 100$ nm), and maximum I_{ON}/I_{OFF} ratio optimized normally for minimum switching delay power product [11]. It is also assumed that both gates have been optimized for symmetrical threshold $V_T = \pm 0.25$ V using a dual-metal process. A generic DG-MOSFET structure based on these design guidelines, and in agreement with the experimentally demonstrated devices [12] is given in Fig. 1(a). 2D simulations of this structure are accomplished using DESSIS [13] in drift-diffusion approximation for carrier transport, which is sufficient for low-power circuit-configurations explored here.

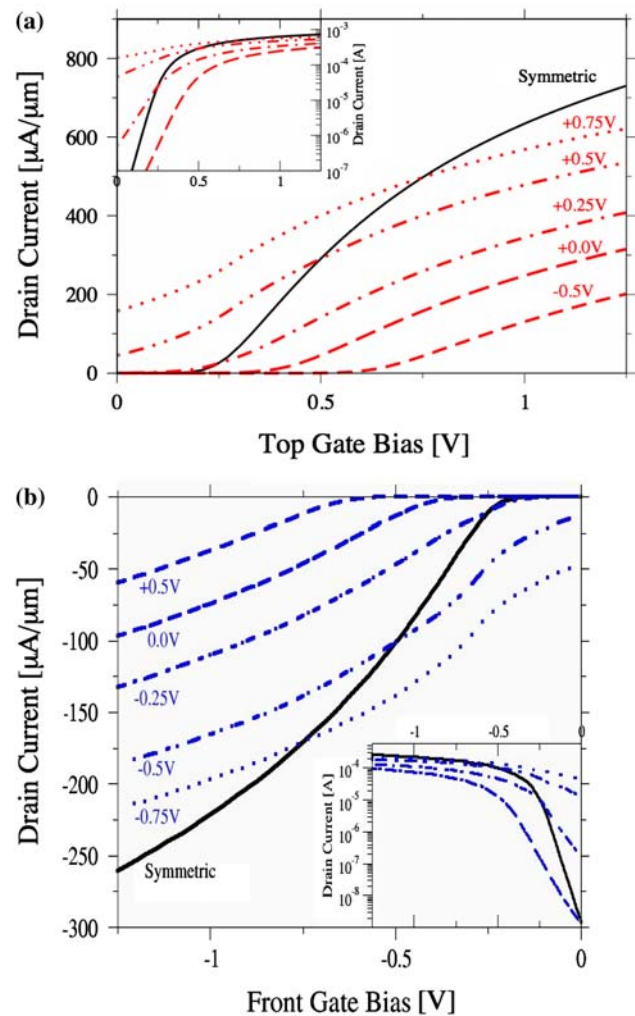


Fig. 2 (a) I_D - $V_{G_{top}}$ characteristics of an *n*-type DG-MOSFETs used for different bottom gate bias conditions. For comparison symmetric ($V_{fg} = V_{bg}$) drive case is also included. Insets show the same data in the semi-log scale. (b) I_D - $V_{G_{top}}$ characteristics of an *p*-type DG-MOSFETs used for different bottom gate bias conditions

Figure 1(b) shows the circuit symbols for both *n*-type and *p*-type DG-MOSFET transistors. A typical transfer curve for an asymmetrically biased *n*-type DG-MOSFET and *p*-type is presented in Fig. 2, where the drain current through the top-gate is studied as a function of bottom gate bias. Clearly, the threshold of individual DG-MOSFETs can be modified using this approach. However, it must be pointed out that the resulting independently driven devices (IDDG) are always inferior to symmetrically driven counterparts (SDDG) in terms of transconductance and sub-threshold performance, under equal geometry and bias conditions. Thus bottom-gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price well justified by variety of circuit possibilities, as explored below.

2 Tunable current mirrors

The simple current mirror (CM) (see Fig. 3(a)) constitutes one of the simplest yet most important design blocks for analog circuit engineering. It can be used to copy reference currents or set operating points across the integrated analog circuit blocks. Normally, depending on the ratio of transistor width between the input (reference) and output

branch, the mirror characteristics can be set, which is constant once the circuit is built. In our case, however, a similar gain factor can be easily obtained, and dynamically changed, by appropriate bottom biases of DG-MOSFETs used in the mirror block, as shown in Fig. 3(b). Tunability not only greatly enhances the variety of applications for this otherwise simple circuit, but could also lead to area and/or power savings over similar circuits built using bulk MOSFETs. Even for the modest bottom-bias conditions at the output transistor ($V_{seto} \leq 1$ V), it is possible to achieve mirror ratios around 100. This can be visualized in Fig. 3(c), plotting the relation between the output current (I_{out}) and output node (V_{out}) for constant I_{in} at different setting voltage (V_{seto}). Alternatively, Fig. 4(a) shows the relation between output current and setting voltage (V_{seto}) for different input currents (I_{in}). The inset of this figure shows the current ratio versus bottom-gate setting voltage.

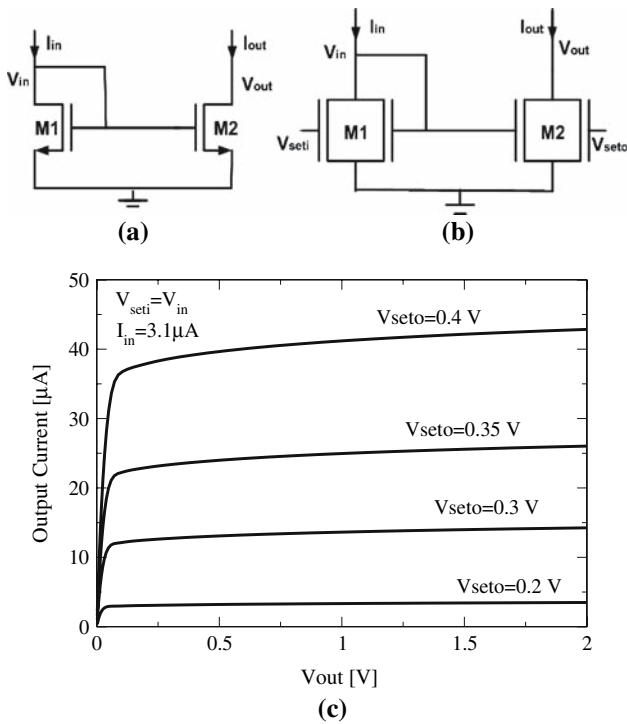


Fig. 3 (a) Simple current mirror based on conventional CMOS transistors. (b) Simple current mirror based on DG-MOSFET. (c) The output current versus output voltage for DG-MOSFET simple current mirror

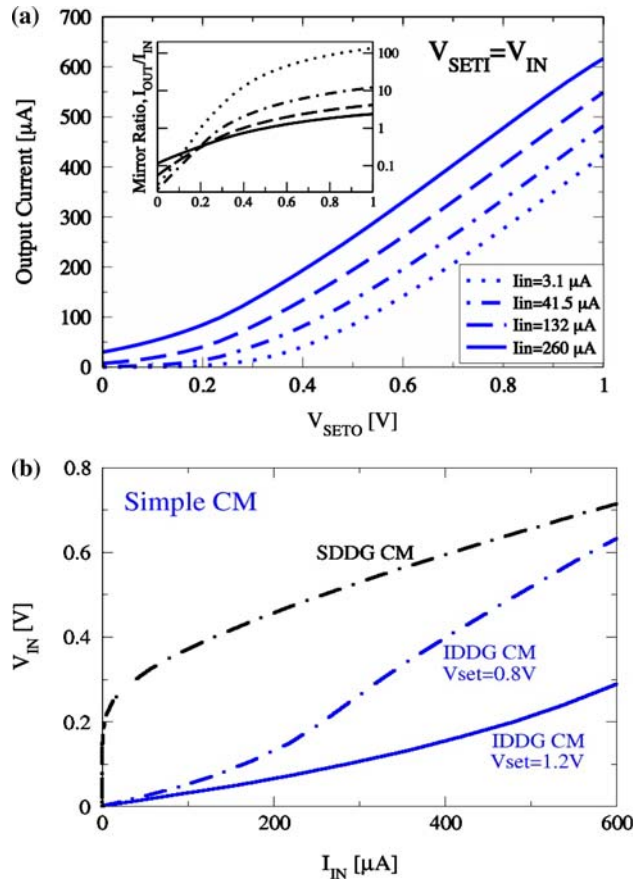


Fig. 4 (a) Output current for different reference voltage V_{ref} (e.g. I_{IN}) versus output setting-voltage (V_{seto}). The inset shows the mirror ration between the output and input stage of the mirror. (b) Comparison of the required voltage across the input transistor of the simple DG current mirror in three configurations: SDDG (conventional: no bottom gate control) and IDDG with two different bias voltages. Higher the bottom gate bias lower the input supply needed

In tunable DG CM circuits, the voltage required across the input DG device mirror is a fraction of that required for conventional MOS current mirror (Fig. 4(b)) simulated in SDDG configuration. Note that output impedance of the simple CM is remarkably lower, while total currents are larger (see Fig. 3(c)), than the previously published examples by Kumar et al. [14]. This previous work was based on long (1 μm) DG-MOSFETs, as opposed to 100 nm devices used here and could not take into account short channel effects accurately due to model limitations. Our TCAD analysis adequately resolves short channel

effects as can be understood by decreasing output resistance. This compromise in output conductance can be easily offset by adapting a modified cascade CM, shown in Fig. 5(a), which is suitable for low-voltage operation. The cascade CM design retains all aspects of tuning in the simple CM while improving output as shown in Fig. 5(b). Moreover, it also does not result in a major drawback for the supply voltage, except a minor increase from simple CM. Once again for comparison, Fig. 6 also contrasts the required voltage across the both input devices (M1 and M2 in series) of cascade IDDG CM to conventional (SDDG) case, indicating the low-voltage (and low-power) potential of the IDDG configuration.

As shown from the simulation results the DG current mirror has major advantages over conventional MOS current mirror such as lower voltage supply and power dissipation (lower V_{IN}) and tunability without the use of an extra transistor (less area and parasitics). Insight gathered on the CM circuits will be valuable for more complicated

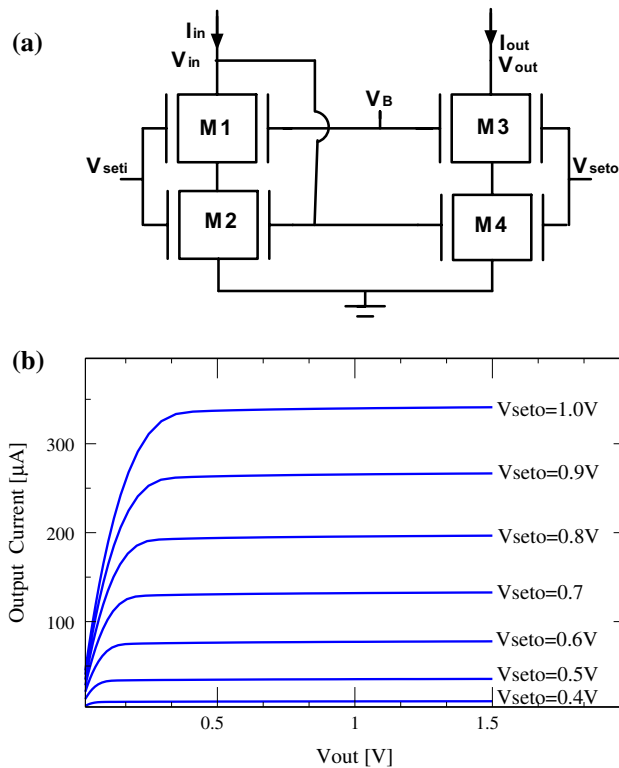


Fig. 5 (a) Cascade current mirror based on DG-MOSFET (b) Output current versus output voltage for DG-MOSFET cascade current mirror at $I_{IN} = 130 \mu\text{A}$ and $V_{seti} = 0.8 \text{V}$

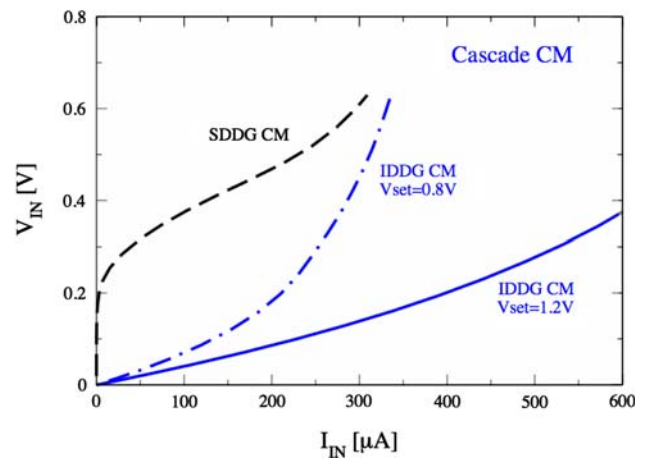
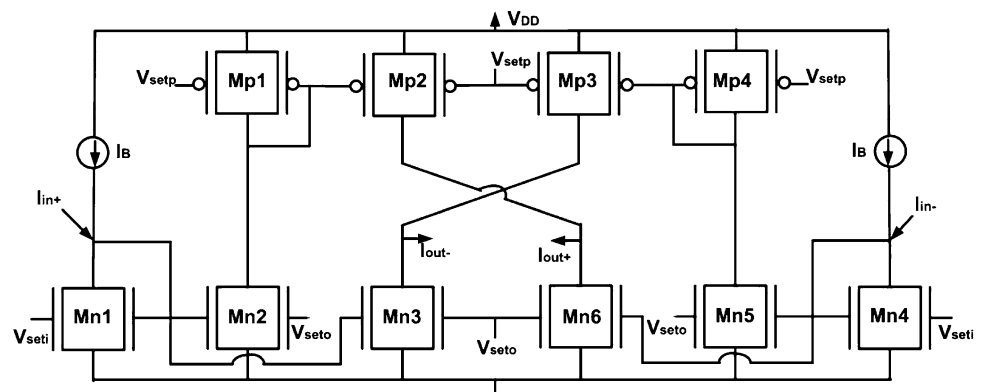


Fig. 6 Comparison of the required voltage across the input transistors of the cascade DG current mirror in three configurations: SDDG (conventional: no bottom gate control) and IDDG with two different bias voltages. Higher the bottom gate bias lower the input supply needed

Fig. 7 DG differential current amplifier



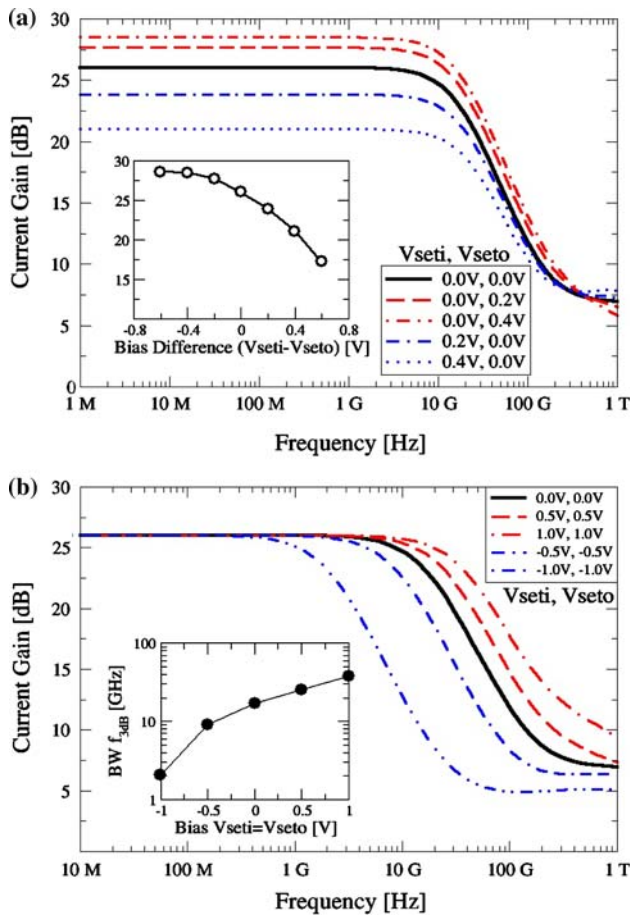


Fig. 8 (a) Gain versus frequency response of the differential current amplifier for various setting voltage pairs ($V_{seti} \neq V_{seto}$). The inset plots the extracted tuning curve for the amplifier. The case for $V_{seti} = V_{seto} = 0.0V$ is also given for comparison. (b) Gain versus frequency response of the differential current amplifier for equal setting voltages ($V_{seti} = V_{seto}$). The inset plots the simulated tuning window for the bandwidth (BW, f_{-3dB}) of the amplifier. Note that the BW may be tuned without change in the gain

current-mode circuits blocks investigated in the following sections, which uses a number of such CM in differential topology to built amplifiers and filters.

3 Turnable current amplifier

The tunable current amplifier is built using two simple DG current mirrors (Mn1,Mn2) and (Mn4,Mn5) as shown in Fig. 7. Where the bottom gates of transistors Mn2 and Mn5 are used for output setting voltage (V_{seto}), while the bottom gates of transistors Mn1 and Mn4 are used for input setting voltage (V_{seti}). PMOS current mirrors (Mp1–Mp4) are used to set output common mode voltage to zero. So it is possible to achieve appreciable gain and bandwidth programming using various biasing schemes

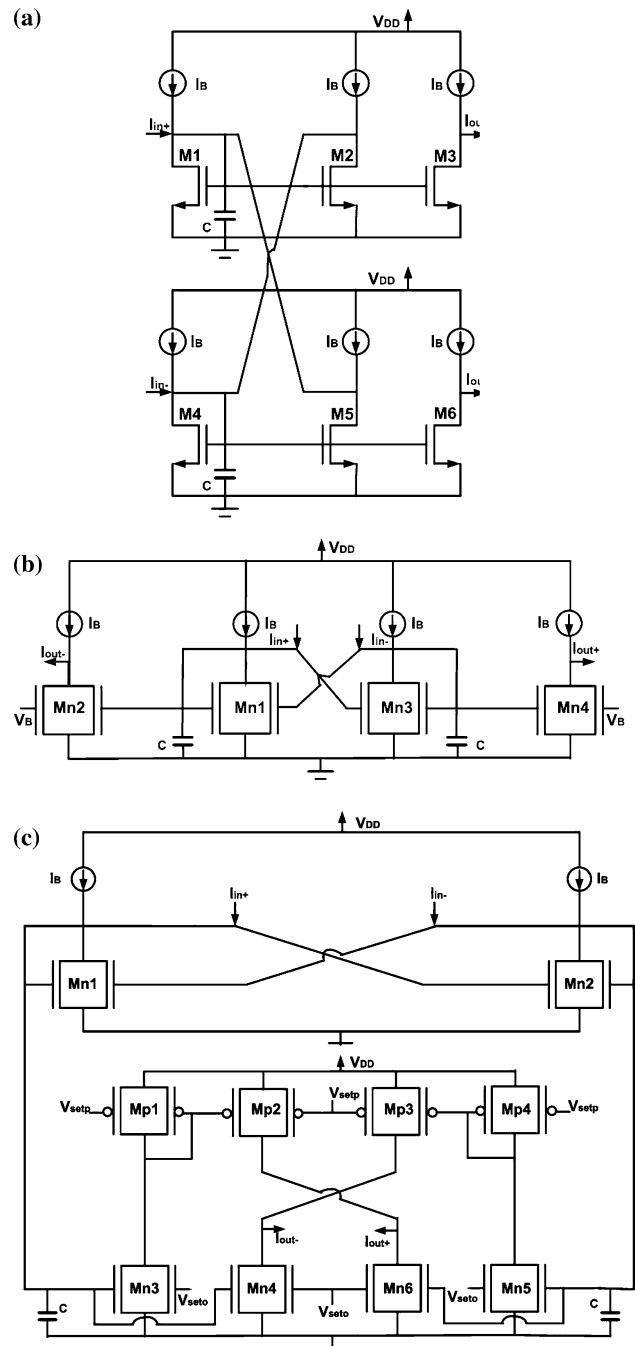


Fig. 9 (a) CMOS differential current integrator. (b) DG differential current integrator. (c) DG differential tunable current integrator

for the bottom-gate control voltages on the input and output sides (V_{seti} , V_{seto}), as shown in Fig. 8(a) and (b). By combining biasing schemes in Fig. 8(a) and (b), it should be possible to tune both gain and bandwidth in a single stage. Once again, this is achieved without the use of extra transistors found in conventional CMOS circuits, thus reducing area, supply and power requirements considerably.

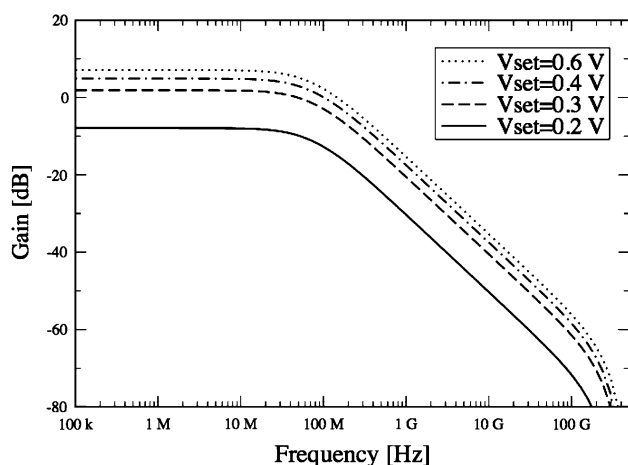


Fig. 10 Gain versus frequency response of the differential current integrator for various setting voltage (V_{set})

4 Current-mode integrator

The proposed current mode fully differential integrator is modified version of the current mode fully differential integrator proposed in [15, 16] (see Fig. 9(a)). As shown in Fig. 9(b) the integrator consists of two DG simple current mirrors. The number of DG transistors used to build the proposed integrator is eight transistors, while the integrator (in Fig. 9(a)) used 12 transistors. In case of using cascade current mirror instead of simple current mirror to improve the performance of the integrator, we will need 16 DG transistors for proposed integrator, instead of 24 transistors needed for conventional CMOS integrator. The tunable current-mode integrator is shown in Fig. 9(c). Where we added the PMOS current mirrors (Mp1–Mp4) to set output common mode voltage to zero during changing the setting voltage (V_{set}). Figure 10 shows the frequency response of the fully differential tunable current integrator for different setting voltage (V_{set}). Where the current ratio between I_{out} and I_{in} can be adjusted by the setting voltage (V_{set}).

5 Conclusions

Unique and novel examples of low-power current mode analog circuit blocks based on DG-MOSFETs have been investigated. Using mixed-mode (device + circuit) TCAD simulations, we have shown how the bottom-gate of independently driven DG-MOSFETs may be used to design and test current mode analog circuits with tunable performance metrics. In particular, we have provided examples for a tunable simple current mirror, a tunable low voltage cascade current mirror, a tunable current amplifier

and a tunable current integrator. The circuits and biasing schemes explored here show how the nano-scale DG-MOSFETs may pave way for efficient, tolerant and smaller circuits with tunable characteristics.

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Hesham F. A. Hamed was born in Giza, Egypt, in 1966. He received the B.Sc. degree in Electrical Engineering, the M.Sc. and Ph.D. degrees in Electronics and Communications Engineering from EL-Minia University, EL-Minia, Egypt, in 1989, 1993, and 1997 respectively. He currently is a Visiting Researcher at Ohio University, Athens, Ohio. From 1989 to 1993 he worked as a Teacher Assistant in the Electrical Engineering Department, EL-Minia University. From 1993 to

1995, he was a visiting scholar at Cairo University, Cairo, Egypt. From 1995 to 1997, he was a visiting scholar at Texas A&M University, College Station, Texas (with the group of VLSI). From 1997 to 2003, he was an Assistant Professor in the Electrical Engineering Department, EL-Minia University. From 2003 to 2005, he was Associate Professor in the same University. He has published more than 30 papers. His research interests include analog and mixed-mode circuit design, low voltage low power analog circuits, current mode circuits, nano-circuits design, and FPGA.



Savas Kaya (M'01) graduated from Istanbul Technical University in 1992 with a B.Sc. in Electronics and Communication Engineering, received M.Phil. degree in 1994 from the University of Cambridge, U.K., and Ph.D. degree in 1998 from Imperial College of Science, Technology & Medicine, London, U.K., for his work on strained Si quantum wells on vicinal substrates. From 1998 to 2001, he was a Postdoctoral Researcher at the University of

Glasgow, Scotland, U.K., carrying out research in transport and scaling in Si/SiGe MOSFETs, and fluctuation phenomena in decanano MOSFETs. He is currently with the Russ College of Engineering, Ohio

University, Athens, OH. He has served as Air Force Office of Scientific Research Summer Faculty Fellow in 2006. He has over 30 journal papers and 45 conference proceedings. His other interests include nanocircuits, TCAD, transport theory, nanostructures, process integration, ionic transport and biomolecular modelling in trans-membrane proteins. Dr. Kaya was a member of the organizing committee for IWCE'7, 2000, and IEEE Nanotech'6, 2006.



Janusz A. Starzyk (SM'83) received the M.S. degree in Applied Mathematics and the Ph.D. degree in Electrical Engineering from Warsaw University of Technology, Warsaw, Poland, in 1971 and 1976, respectively. From 1977 to 1981, he was an Assistant Professor at the Institute of Electronics Fundamentals, Warsaw University of Technology. From 1981 to 1983, he was a Post-doctorate Fellow and Research Engineer at McMaster University, Hamilton,

ON, Canada. In 1983, he joined the Department of Electrical and Computer Engineering, Ohio University, Athens, where he is currently a Professor of Electrical Engineering and Computer Science. He has cooperated with the National Institute of Standards and Technology in the area of testing and mixed signal fault diagnosis. He has been a consultant for AT&T Bell Laboratories, Sarnoff Research, Sverdrup Technology, Magnolia Broadband, and Magnetek Corporation. His current research is in the areas of self-organizing learning machines, neural networks, rough sets, VLSI design and test of mixed signal complementary metal-oxide-semiconductor (CMOS) circuits, and reconfigurable design for wireless communication.